Power Integrity Engineering
DC Power Integrity

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Power Integrity Engineering

- **Divided into Four Areas**
  - DC Power Integrity
  - Mechanical Contact Integrity
  - Thermal Power Integrity
  - AC Power Integrity
- **We will discuss DC Power Integrity today**

DC Power Integrity…Why Should You Care?

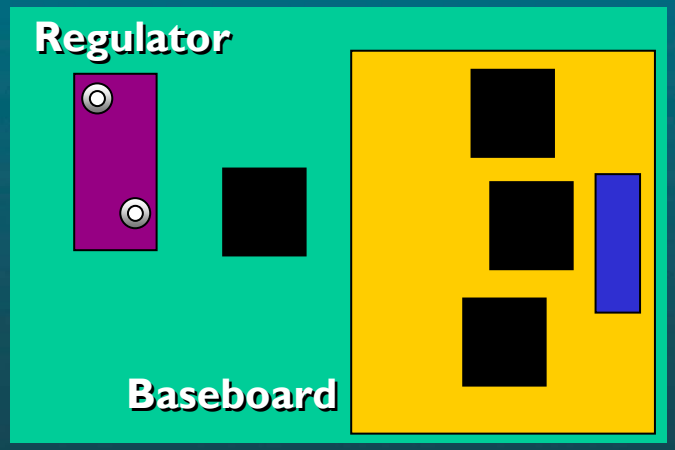
- **Margin, margin, margin!**
  - **Voltage loss margin**
  - **Timing margin**
- **Parts cost**
  - **Connectors**
    - Over design costs space and $
  - **DC regulation**
    - On baseboard versus on module
    - Where to place voltage sense point?

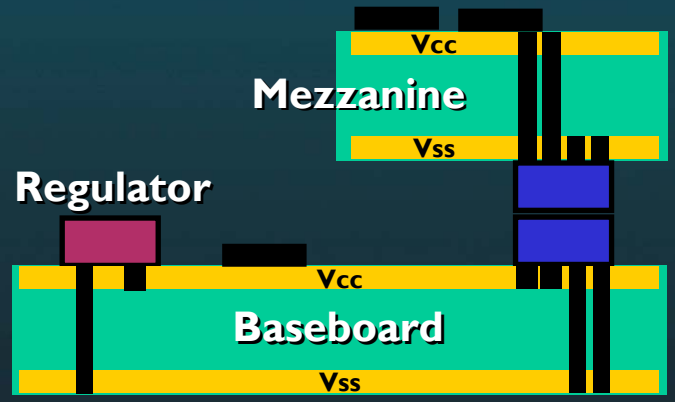
Two Pieces to DC Power Integrity

- **Connector**
  - **Low Level Contact Resistance**
  - **Current @ 30 C temperature rise**
- **PCB**
  - **DC path resistance**
    - Connector BOR
    - Location Dependence
    - Plane Weight
    - PTH versus Surface Mount Pads

Typical DC Power Delivery Application

- DC power delivery loop
  - Regulator Vcc vias
  - Baseboard Vcc plane(s)
  - Connector Vcc vias
  - Baseboard Connector Vcc pins
  - Mezzanine connector Vcc vias
  - Mezzanine Vcc plane(s)
  - IC Vcc vias
  - IC Vss vias
  - Mezzanine Vss plane(s)
  - Mezzanine connector Vss vias
  - Connector Vss pins
  - Baseboard Connector Vss vias
  - Baseboard Vss plane(s)
  - Regulator Vss vias





Mezzanine card with components mounted above baseboard.

DDR3 Power Delivery

- **DDR3-1600**
  - **1.5 V Nominal voltage**
    - +/-3% voltage regulator worst case ΔVo(total)
    - -2% resistive drop (30 mV)
  - **64 bit bus with eight 8-bit components**
  - **600 mA Idd7 per component**
  - **4.8 A total DC current**

- **DC power delivery loop**
  - Regulator Vcc vias
  - Baseboard Vcc plane(s)
  - Connector Vcc vias
  - Baseboard Connector Vcc pins
  - Mezzanine connector Vcc vias
  - Mezzanine Vcc plane(s)
  - IC Vcc vias
  - IC Vss vias
  - Mezzanine Vss plane(s)
  - Mezzanine connector Vss vias
  - Connector Vss pins
  - Baseboard Connector Vss vias
  - Baseboard Vss plane(s)
  - Regulator Vss vias

6.25 mΩ total Vcc/Vss path loss allowed for 30 mV resistive drop

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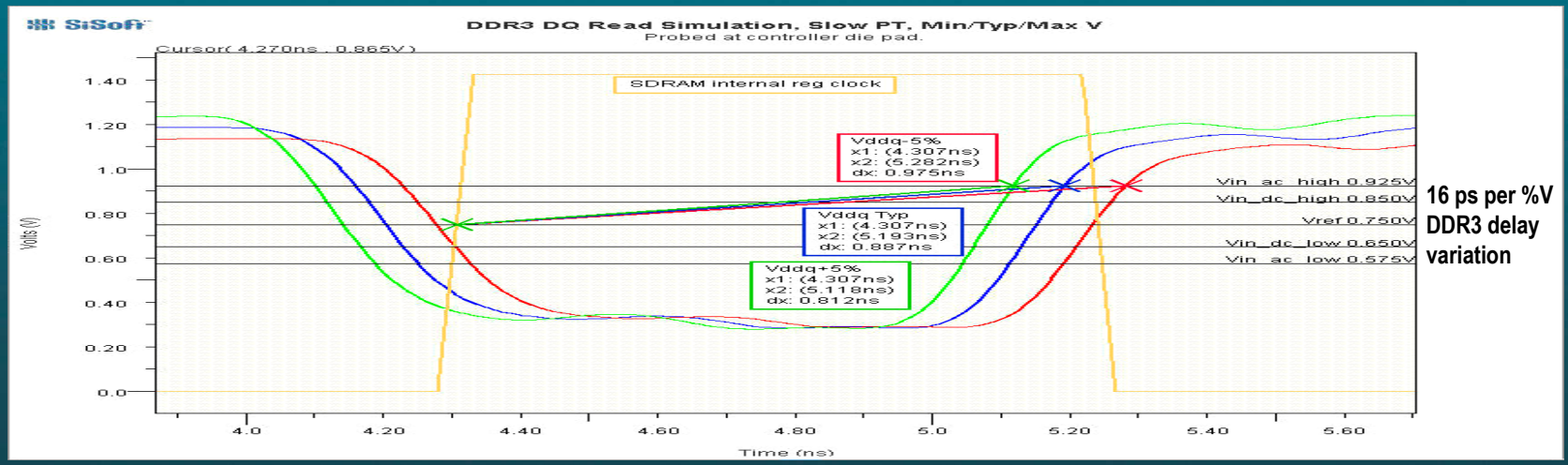
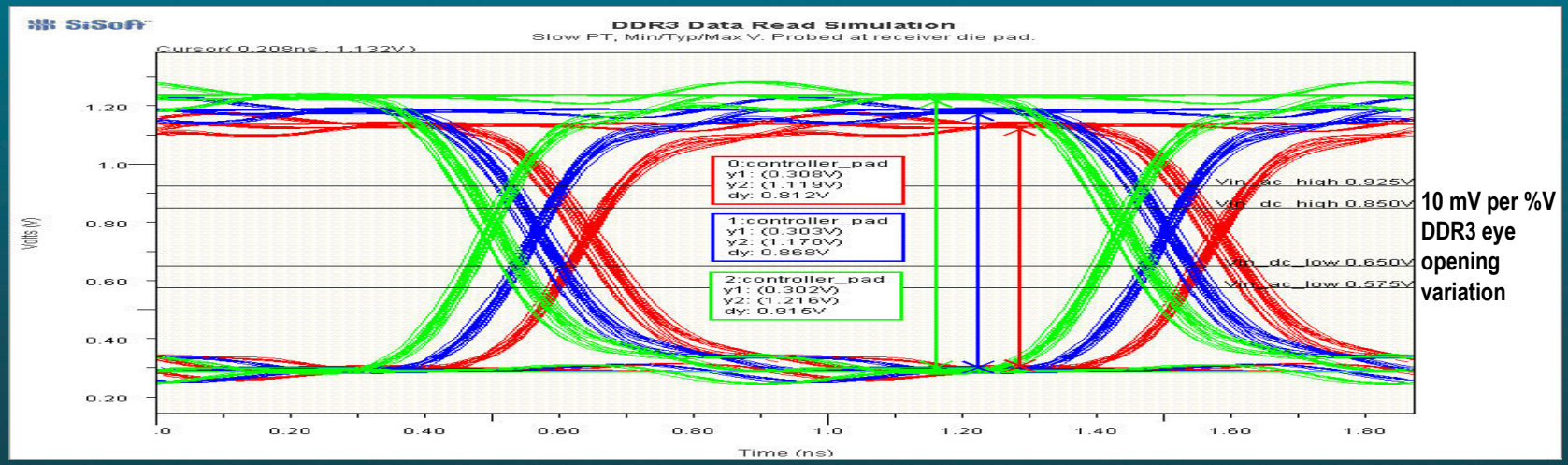
DC Voltage Impact on Output Delay VCC = 1.5 V +/- 5%



16 ps per %V DDR3 delay variation

- **DC voltage variation causes a noticeable change in output delay (Tco).**
  - **May not be an issue for source synchronous busses**
    - But will definitely impact all internal device speeds
  - **Several design choices**
    - Design to DC minimum margin
      - Does not allow for additional AC power droop
      - Meets minimum device specifications
    - Design DC power delivery system to be better than minimum
      - Increase overall design margins
      - Relatively free performance improvement

DC Voltage Impact on Data Eye Margin VCC = 1.5 V +/- 5%



- **Eye opening margin is directly proportional to average DC voltage.**
  - **Robust engineering of the DC power path leads to increased overall signal voltage margins**
    - Any improvement over absolute DC minimum specified voltage is a free performance improvement
- **Analysis of the DC power delivery system is key.**

Fundamental DC Power Integrity Resistance Calculations

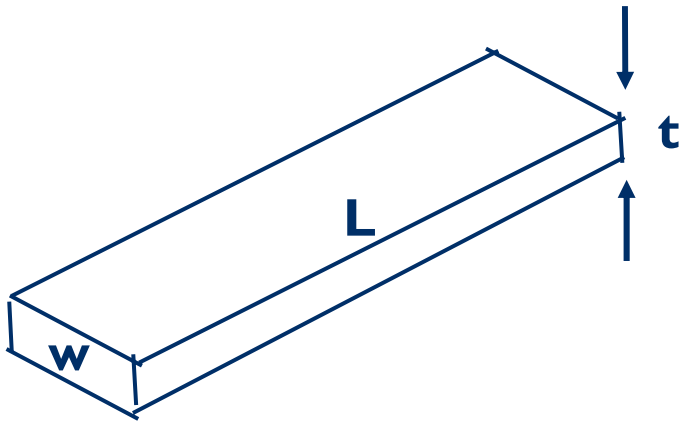
- **Simple problems can be solved from first principals.**
  - **Resistance of a trace**
  - **Resistance of a via**
  - **Spreading resistance between two via contacts on a plane**

Resistance of Traces

$$R = \rho \times {}^{L}\!/_{A}$$

$$A = w \times t$$

$$R = \rho \times {}^{L}\!/_{(w \times t)}$$



where :

$\rho = 6.787e^{-7}\,\text{ohm} - \text{in}$

$L = \text{trace length (in)}$

$A = \text{cross - sectional area (in}^2\text{)}$

$w = \text{trace width (in)}$

$t = \text{trace thickness (in)}$

Resistance of a Via

$$R = \rho \times L/A$$

$$A = \pi \times (d + t) \times t$$

$$R = \rho \times \frac{L}{(\pi \times (d + t) \times t)}$$

where :

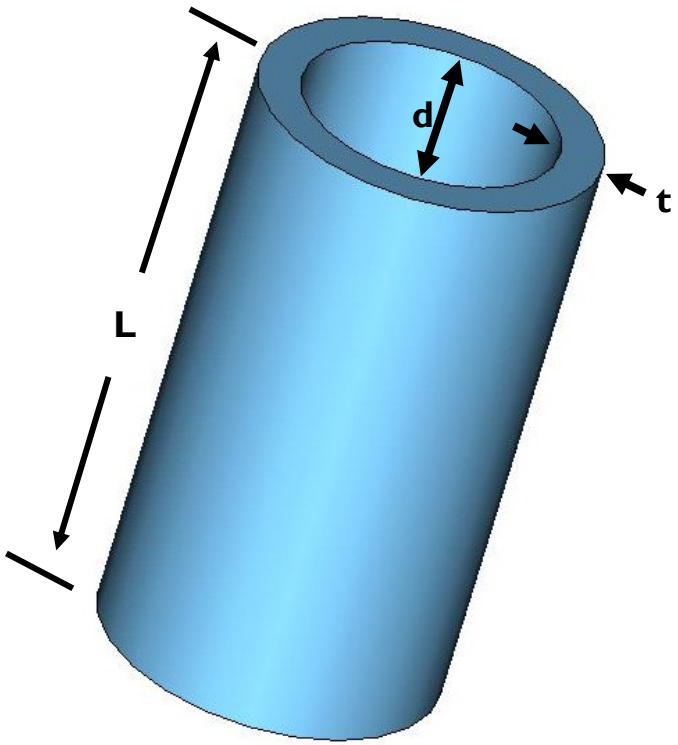
$\rho = 6.787e^{-7}\,\text{ohm} - \text{in}$

L = via length (in)

$A = \text{cross - sectional area } (\text{in}^2)$

t = via plating thickness (in)

d = via inside diameter (in)



Spreading Resistance of Via Contacts on Copper Planes

$$R = \frac{\rho}{2\pi \times t} \times \left(\int_{r1}^{S} \frac{1}{r} + \int_{r2}^{S} \frac{1}{r} \right)$$

$$R = \frac{\rho}{2\pi \times t} \times \left(\ln\left(\frac{s}{r_1}\right) + \ln\left(\frac{s}{r_2}\right) \right)$$

where :

$\rho = 6.787e^{-7} ohm - in$

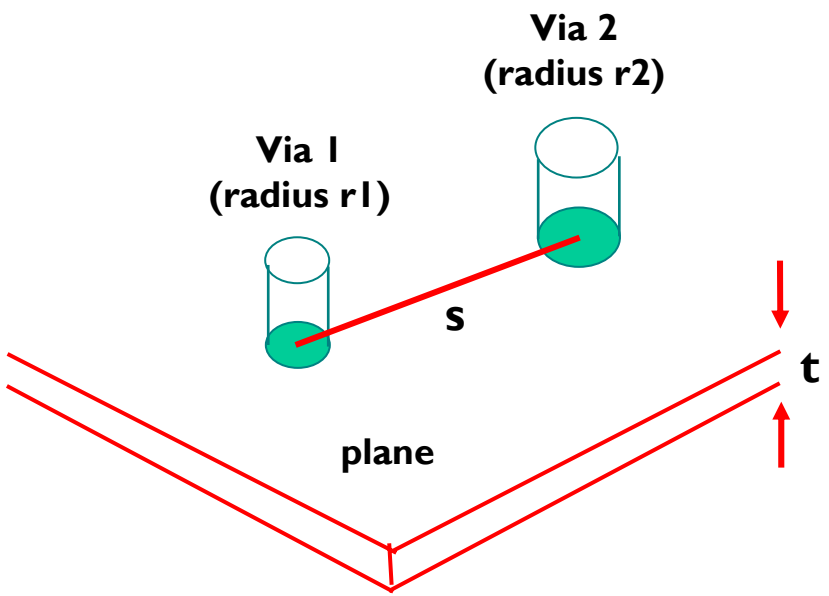
s = center - to - center spacing (in)

t = thickness (in)

r1 = via 1 radius

r2 = via 2 radius

S >> r1, r2, and plane is larger

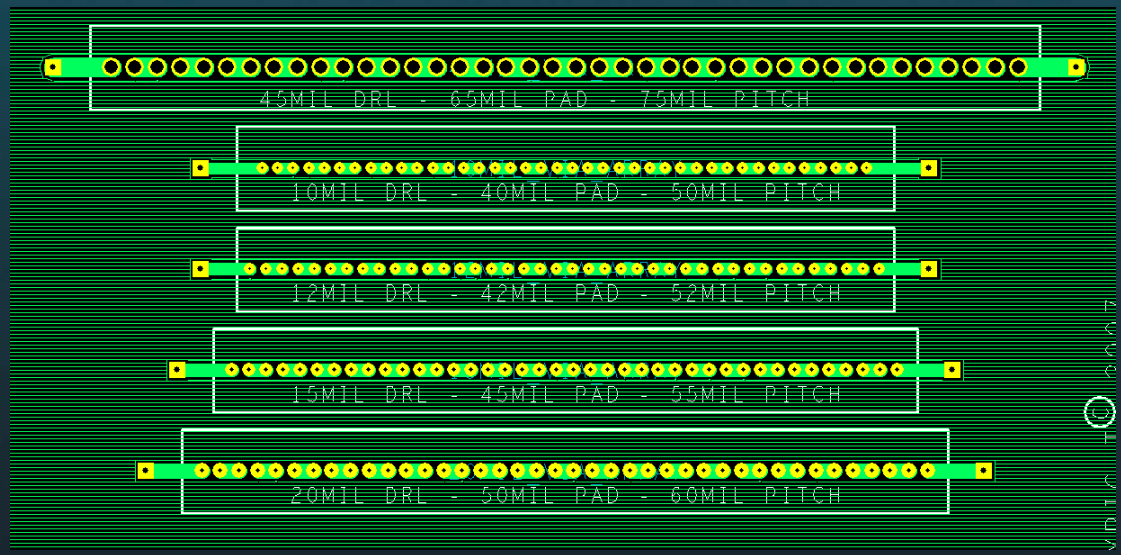


Analytical Calculations versus Solver

- **Analytical Calculations**
  - **Quick and simple**
  - **Accurate for well-defined cases**
    - Vias, traces, large planes
  - **Hard to use with complex geometries**
    - Multiple vias, vias attached to large fill areas, odd shaped planes, cutout/void regions
- **DC FEM Resistance Solvers**
  - **Accurate for complex cases**
  - **Expensive**

Power Integrity Guidelines Correlation Test Structures

- **Serial Via Resistance**
  - **Arrays of 40 vias with 45, 20, 15, 12, and 10 mil finished hole diameter are available for the accurate measurement of average via resistance, with the inclusion of attach traces**
  - **Also used for the accurate adjustment of PCB fabrication parameters**
    - Copper thickness
    - Via barrel plating thickness

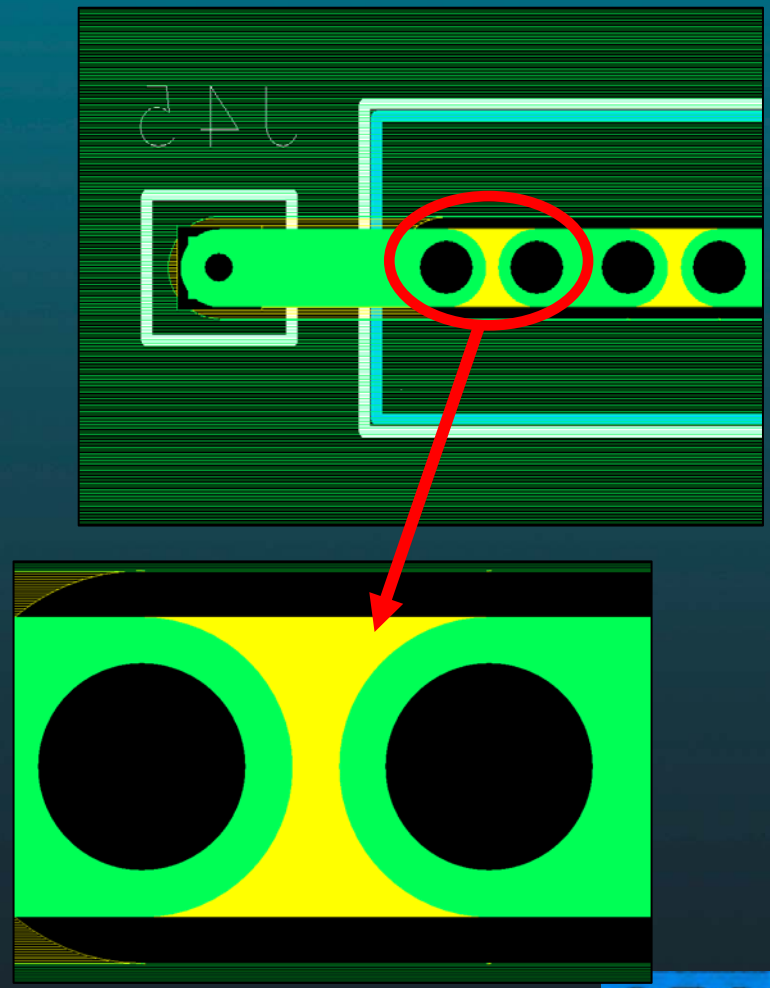


FWJ/FHP Power Integrity Guidelines Documentation Goals

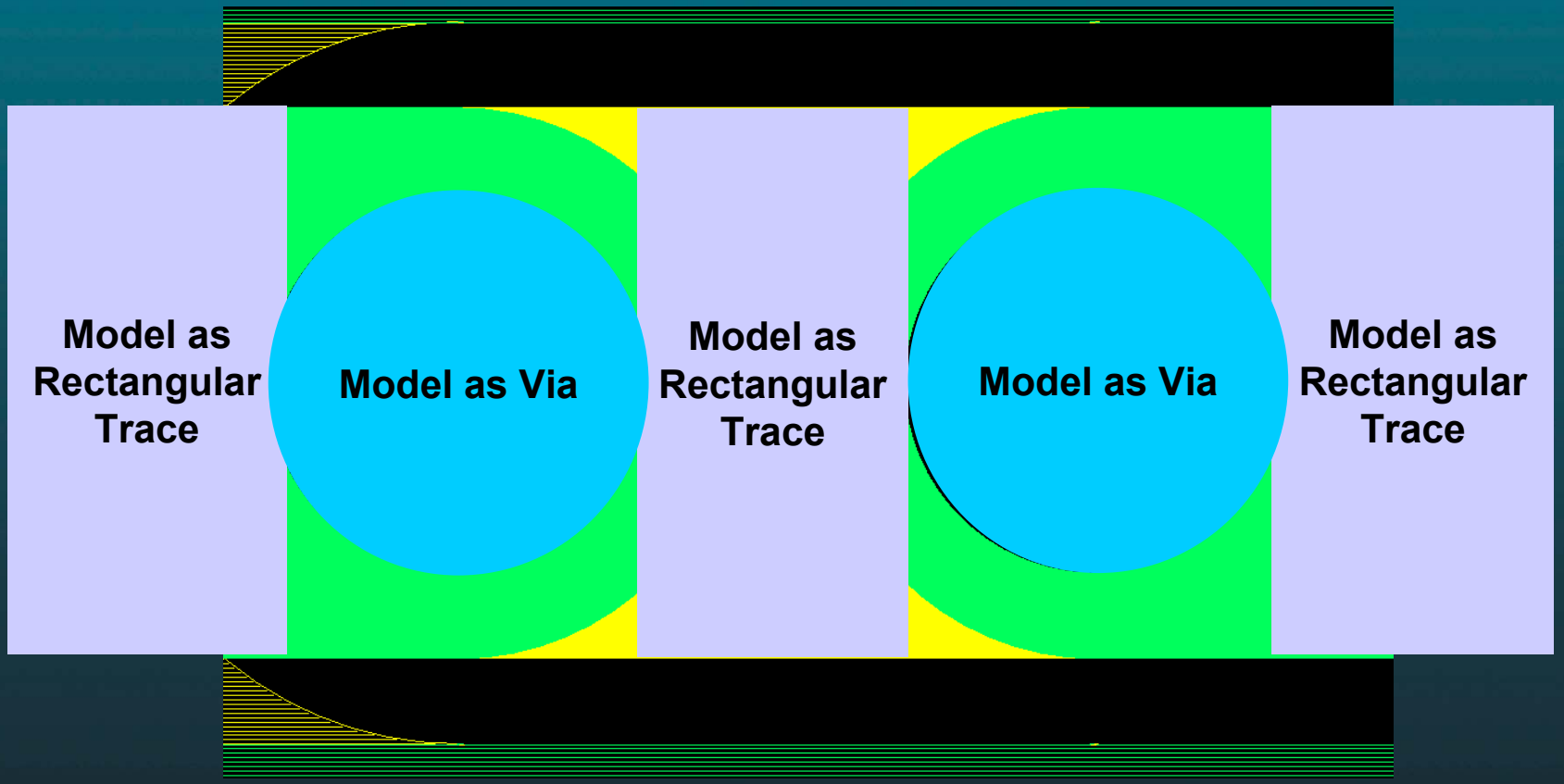
- **Provide Information for:**
  - **DC characterization of the power blades of the connector system**
    - Include mounted breakout resistivity
    - Include via resistivity
    - Correlate simulation to measurements

Model/Simulator Validation

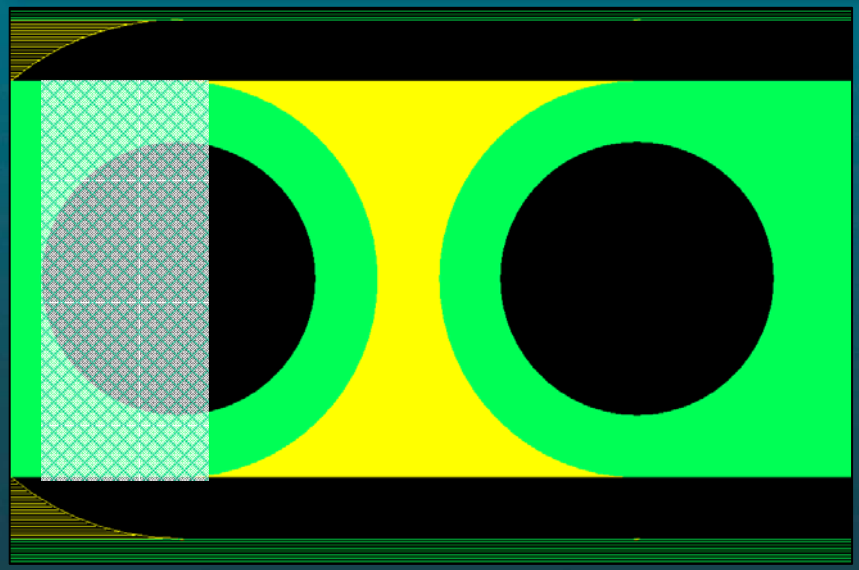
- Via test strip contains
  - 40 - 45 mil vias
  - 39 – trace connections between vias
  - 2 – trace connections from test point to via array
  - 40 – Via/Trace overlaps
- 40 Vias
  - 45 mil hole
  - 1.65 mil plating
- 39 Via-to-via trace connections
  - 65 mil trace width
  - 2 mil trace thickness
  - 30 mil trace length
- 2 Test point-to-via trace connection
  - 65 mil trace width
  - 2 mil trace thickness
  - 143 mil trace length
- 40 Via/Trace overlaps
  - 40 via/trace overlapping areas
  - Via increases effective trace resistance

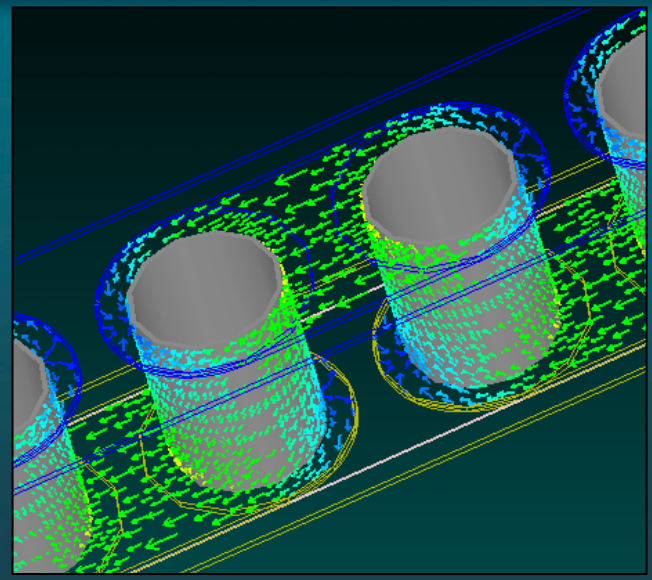


Simplified Incremental Modeling of Vias Connected by Traces



Via/Trace Overlap Model Approximation





- Model as a trace and then scale for surface area lost
- Assume that negligible current flows on far side of via trace
  - This assumption is confirmed by 3D finite element simulation
  - Resistance of Trace = Resistivity x length/Area
  - Surface Area of Trace = Via Inner Diameter x Via Pad Diameter / 2
  - Surface Area of Via Hole = π x Via Diameter ^{2} / 2
  - Scale Factor = (Surface Area of Trace – Surface Area of Via Hole) / Surface Area of Trace

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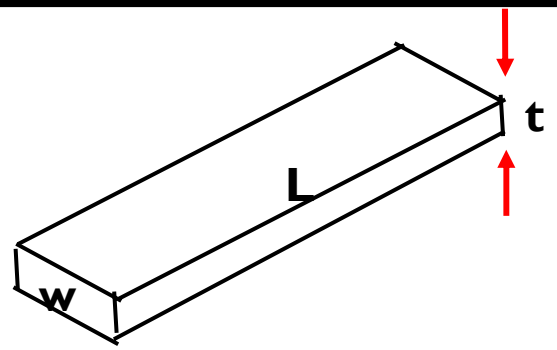
Via-to-Via Trace Resistance Calculation

- **The resistance of a trace can be calculated by the following standard formula:**
  - **Trace Resistance = Resistivity x Length of trace / Area of trace**
  - **Area = Trace Width x Total Thickness (copper + plating)**
  - **Resistivity of Copper = 1.7e-6 Ω-cm (.67e-6 Ω-in)**
    - For a 30 mil long trace, 65 mil wide, with 2 mil thickness
    - Trace Resistance = .67E-6 x .030 / (.065 x .002)
    - Trace Resistance = 154 μΩ



$$R = \rho \times L/A$$

$$A = w \times t$$

$$R = \rho \times L/(w \times t)$$

where:

$\rho = 6.787e^{-7} \text{ohm} - \text{in}$

L = trace length (in)

A = cross-sectional area (in^2)

w = trace width (in)

t = trace thickness (in)

Via Resistance Calculation

- **The resistance of a via can be approximated by calculating the resistance of the equivalent rectangular volume described by:**
  - **Via Resistance = Resistivity x Length of Via / Area of Via Plating**
  - **Area = pi x (Inner diameter + Plating thickness) x Plating thickness**
  - **Resistivity of Copper = 1.7e-6 Ω-cm (.67e-6 Ω-in)**
    - For a 45 mil via hole 62 mils long with 2 mil plating
    - Via Resistance = .67E-6 x .062 / π x (.045 + .002) x .002
    - Via Resistance = 141 μΩ

$$R = \rho \times L/A$$

$$A = \pi \times (d + t) \times t$$

$$R = \rho \times \frac{L}{(\pi \times (d + t) \times t)}$$

where :

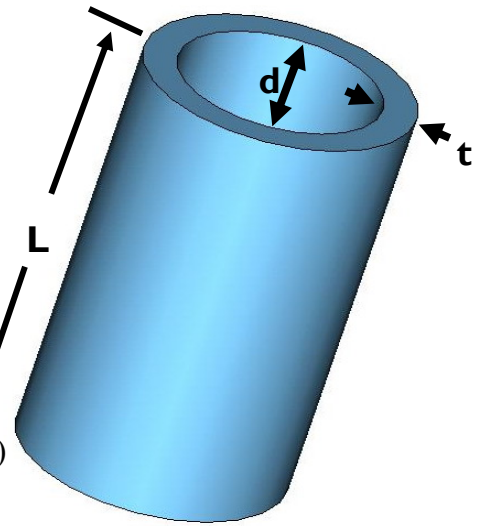
$\rho = 6.787e^{-7}\ ohm - in$

$L = via\ length\ (in)$

$A = cross\text{-}sectional\ area\ (in^2)$

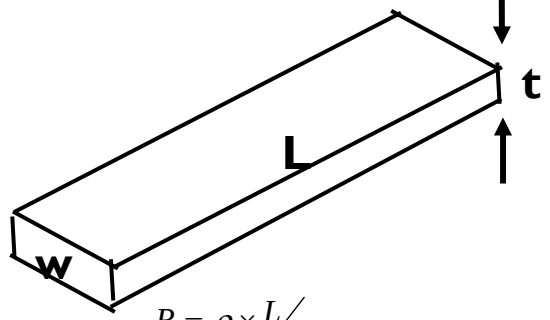
$t = via\ plating\ thickness\ (in)$

$d = via\ inside\ diameter\ (in)$



Test Point-to-Via Trace Resistance Calculation

- **The resistance of a trace can be calculated by the following standard formula:**
  - **Trace Resistance = Resistivity x Length of trace / Area of trace**
  - **Area = Trace Width x Total Thickness (copper + plating)**
  - **Resistivity of Copper = 1.7e-6 Ω-cm (.67e-6 Ω-in)**
    - For a 143 mil long trace, 65 mil wide, with 2 mil thickness
    - Trace Resistance = .67E-6 x .143 / (.065 x .002)
    - Trace Resistance = 737 μΩ



$$R = \rho \times L/A$$

$$A = w \times t$$

$$R = \rho \times L/(w \times t)$$

where :

$\rho = 6.787e^{-7}\,\text{ohm} - \text{in}$

$L = \text{trace length (in)}$

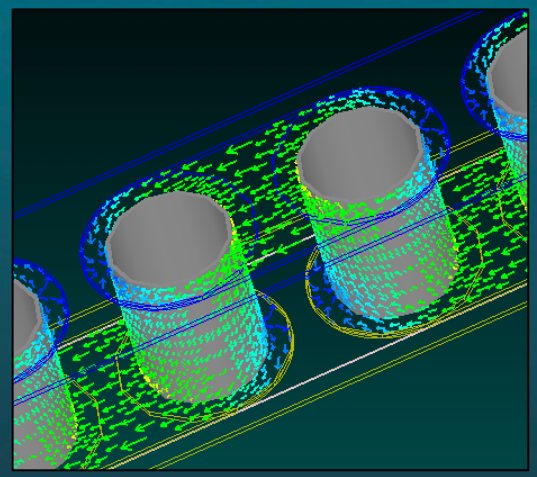
$A = \text{cross - sectional area } (\text{in}^2)$

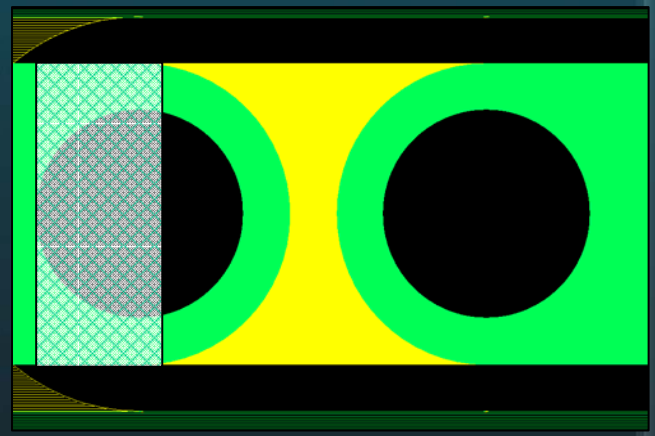
$w = \text{trace width (in)}$

$t = \text{trace thickness (in)}$

Via/Trace Overlap Resistance Calculation

- **The resistance of a trace can be calculated by the following standard formula:**
  - **Trace Resistance = Resistivity x Length of trace / Area of trace**
  - **Area = Trace Width x Total Thickness (copper + plating)**
  - **Resistivity of Copper = 1.7e-6 Ω-cm (.67e-6 Ω-in)**
    - For a 22.5 mil long trace, 65 mil wide, with 2 mil thickness
    - Trace Resistance = .67E-6 x .0225 / (.065 x .002)
    - Trace Resistance = 116 μΩ
    - Surface Area of Trace = .045 x .065/2 = 1.4625e-3
    - Surface Area of Via Hole = π x (.045/2) 2 /2 = .795e-3
    - Scale Factor = (1.4625e-3 – .795e-3) / 1.4625e-3 = .458
    - Resistance = 253 μΩ





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45 mil Via Test Array Resistance Calculation

- **The resistance of the via array is calculated as follows:**
  - **40 Vias**
    - 40 x 141 μΩ = 5.64 mΩ (24%)
  - **39 Via-to-via trace connections**
    - 39 x 154 μΩ = 6.01 mΩ (26%)
  - **2 Test point-to-via trace connection**
    - 2 x 737 μΩ = 1.47 mΩ (6%)
  - **40 Via/Trace overlaps**
    - 40 x 253 μΩ = 10.12 mΩ (44%)
    - Total 23.24 mΩ (100%)

Key Point: Breakout traces attached to vias contribute 75% of the via resistance.

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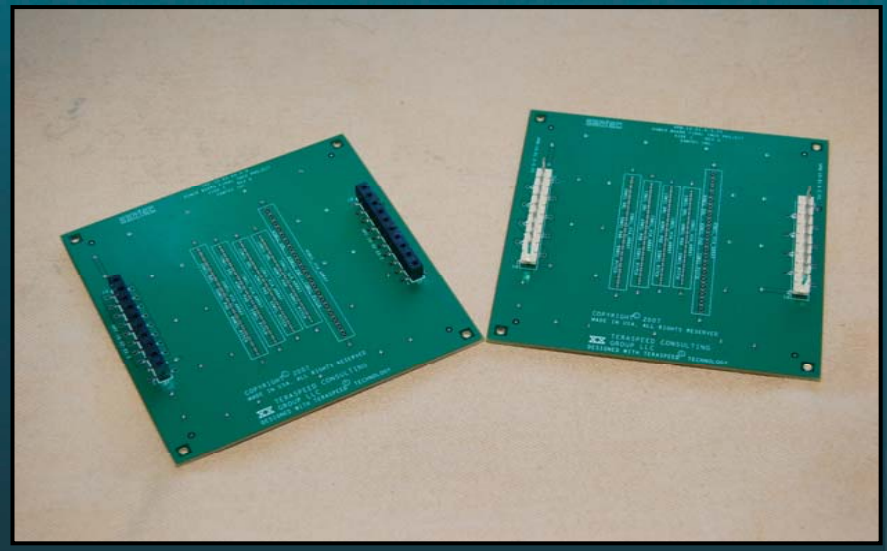
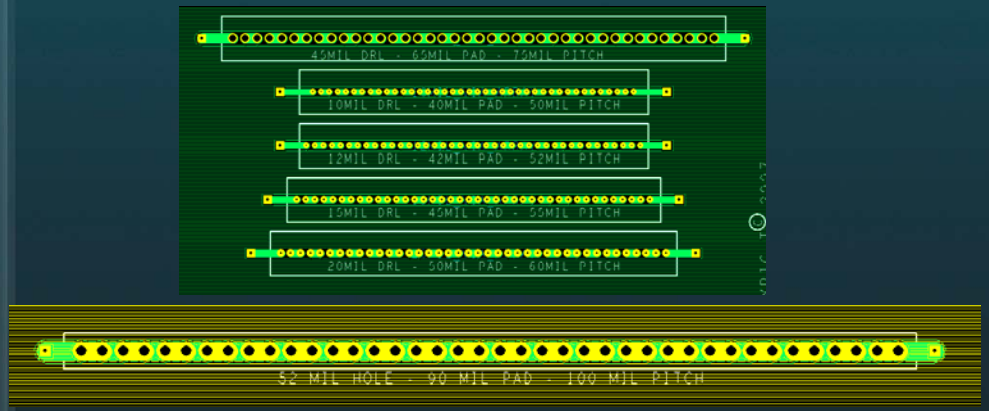
Power Integrity Test Board Sets



Measurement to Solver Correlation of Via Array Resistance

Via	40 Via Resistance Measured	40 Via Resistance Simulated Ansoft SIWave	Average Linear Via Interconnect Resistance	Ansoft Extracted Via Barrel Resistance	Residual non-Via Interconnect Resistance
52 mil	21.9 mΩ	19.38 mΩ (19.9 by hand)	510 µΩ	159 µΩ	351 µΩ
45 mil	21.9 mΩ	21.8 mΩ (23.2 by hand)	510 µΩ	159 µΩ	351 µΩ
20 mil	32.3 mΩ	33.6 mΩ	770 µΩ	401 µΩ	369 µΩ
15 mil	43.7 mΩ	44.2 mΩ	1.06 mΩ	647 µΩ	413 µΩ
12 mil	47.3 mΩ	47.3 mΩ	1.15 mΩ	704 µΩ	446 µΩ
10 mil	48.0 mΩ	49.1 mΩ	1.16 mΩ	729 µΩ	431 µΩ



Linear Via Interconnect Resistance – the resistance of the via barrel, pad, and connecting trace calculated by removing the test trace resistance from the 40 via measured resistance and dividing by 40.

Via Barrel Resistance – the resistance of the via barrel by itself.

Residual non-via interconnect resistance – the resistance of the pad and connecting trace for one via calculated by subtracting the barrel resistance from the linear resistance.

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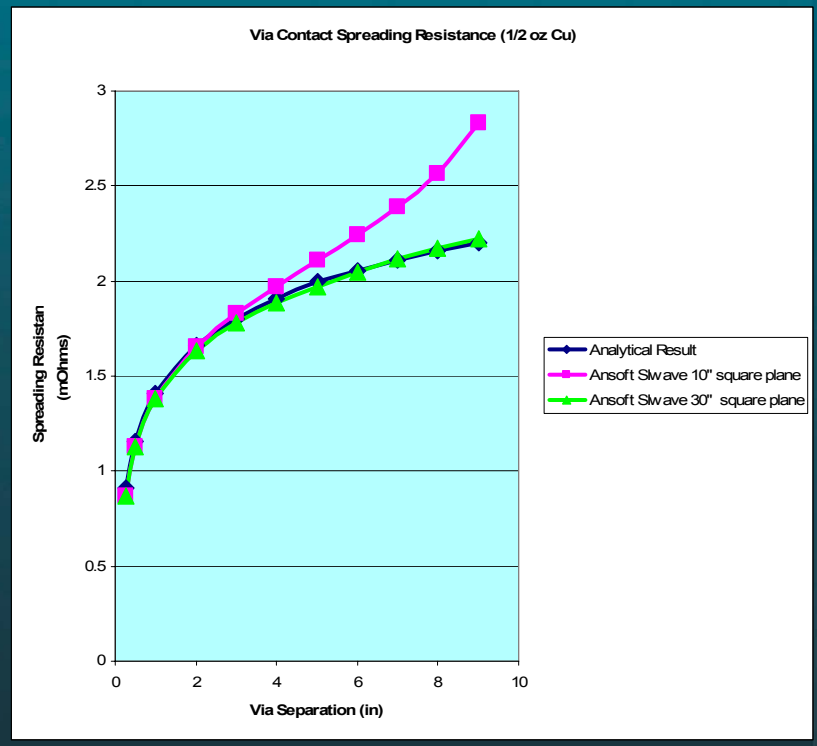
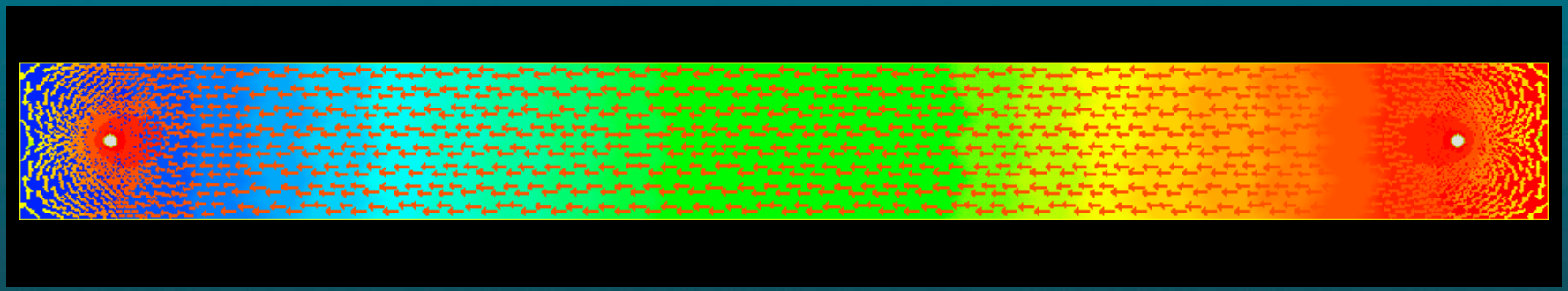
Spreading Resistance Example

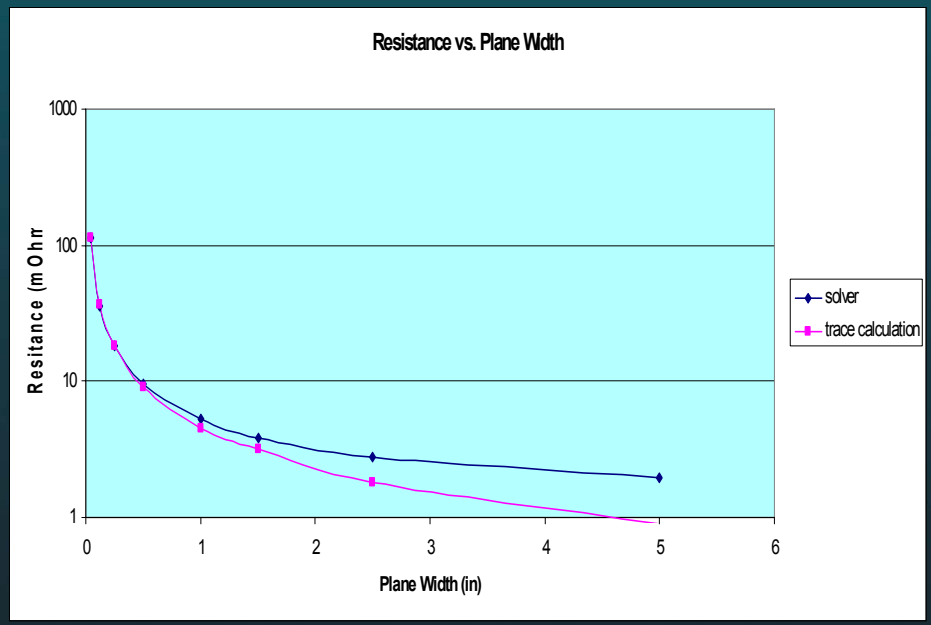
- Analytical formula for spreading resistance between via contacts assumes an infinite plane.
- When the plane is finite, current density increases as via separation/PCB size increases above 1/3.
- Increased current density causes a subsequent increase in resistance between contacts.
- Analytical formulas are good … until the fundamental assumptions are broken, or the cases become too complex.
  - Commercial finite element resistive solvers, such as Ansoft Slwave can be used to perform accurate numerical solutions



Contact Resistance versus Strip Width
40 mil Contact Vias



- Analytically approximate as the resistance of a large trace.
- Solutions converge when strip width is <10X via contact diameter.
- Via contact size limits current flow (increases resistance).
- Number of vias used and size is important.



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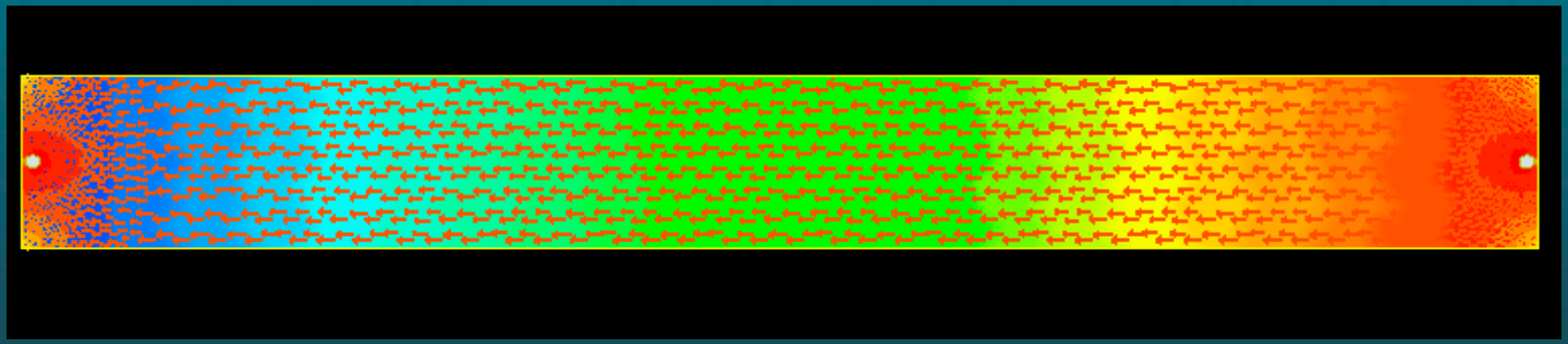
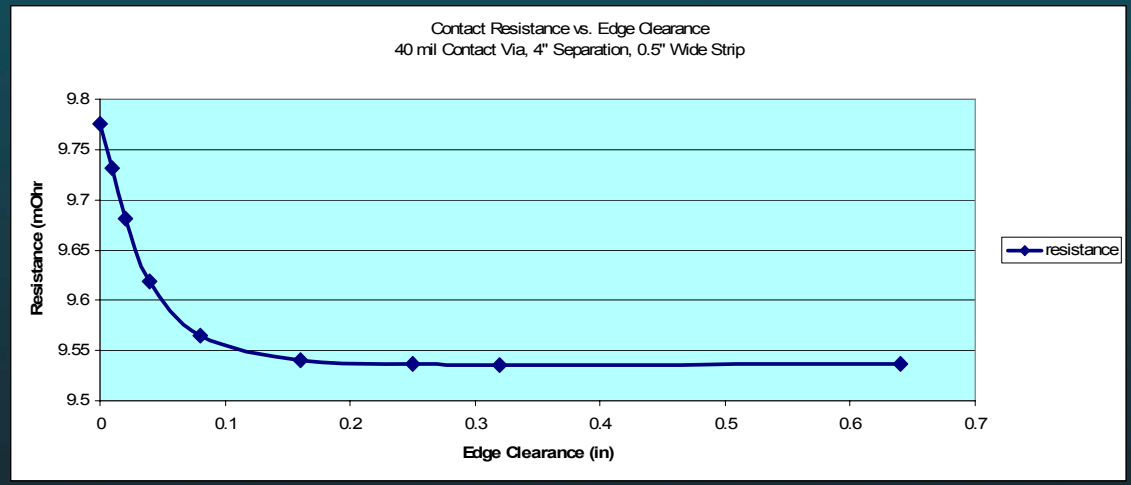
Contact Resistance versus Clearance
40 mil Contact Vias, 0.5” wide strip



- As the via contacts approach the edge of the strip/plane, local current density increases, and resistance increases.
- Negligible increase when clearance is >3X via contact diameter.



Power fill area width makes a huge difference in resistance

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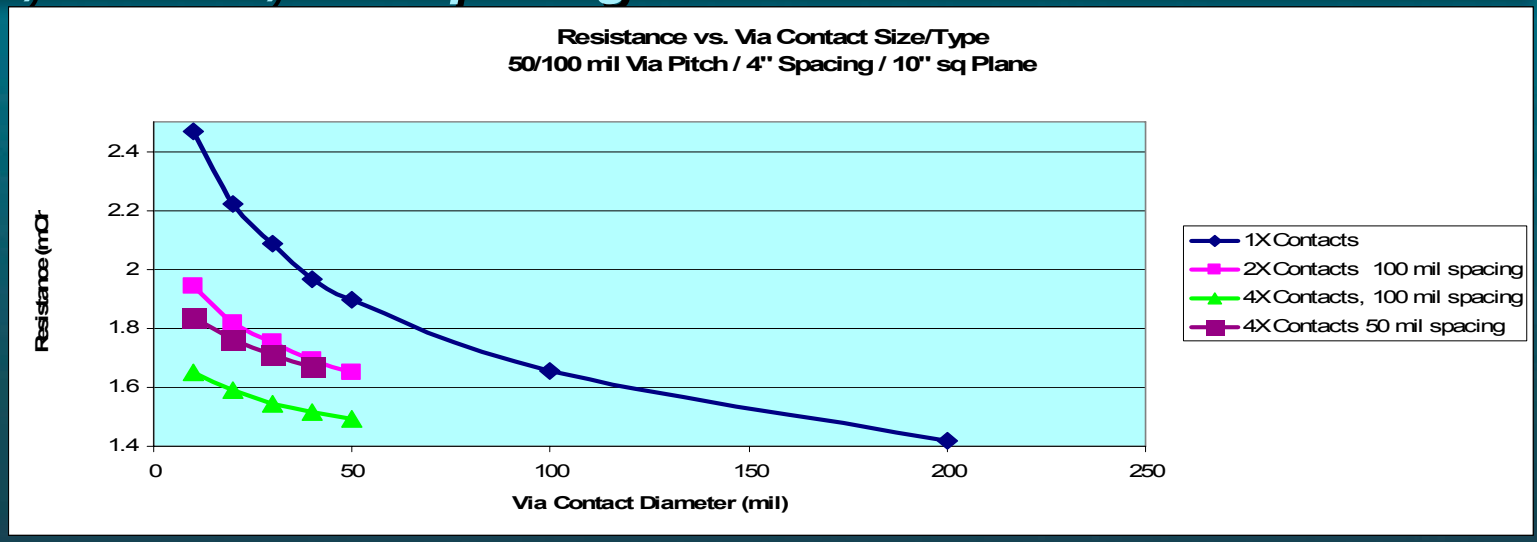
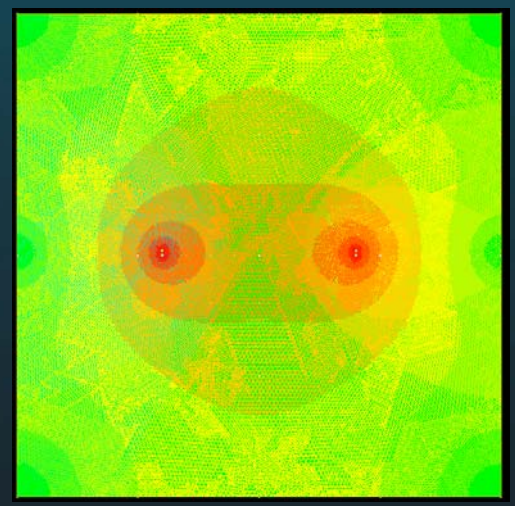
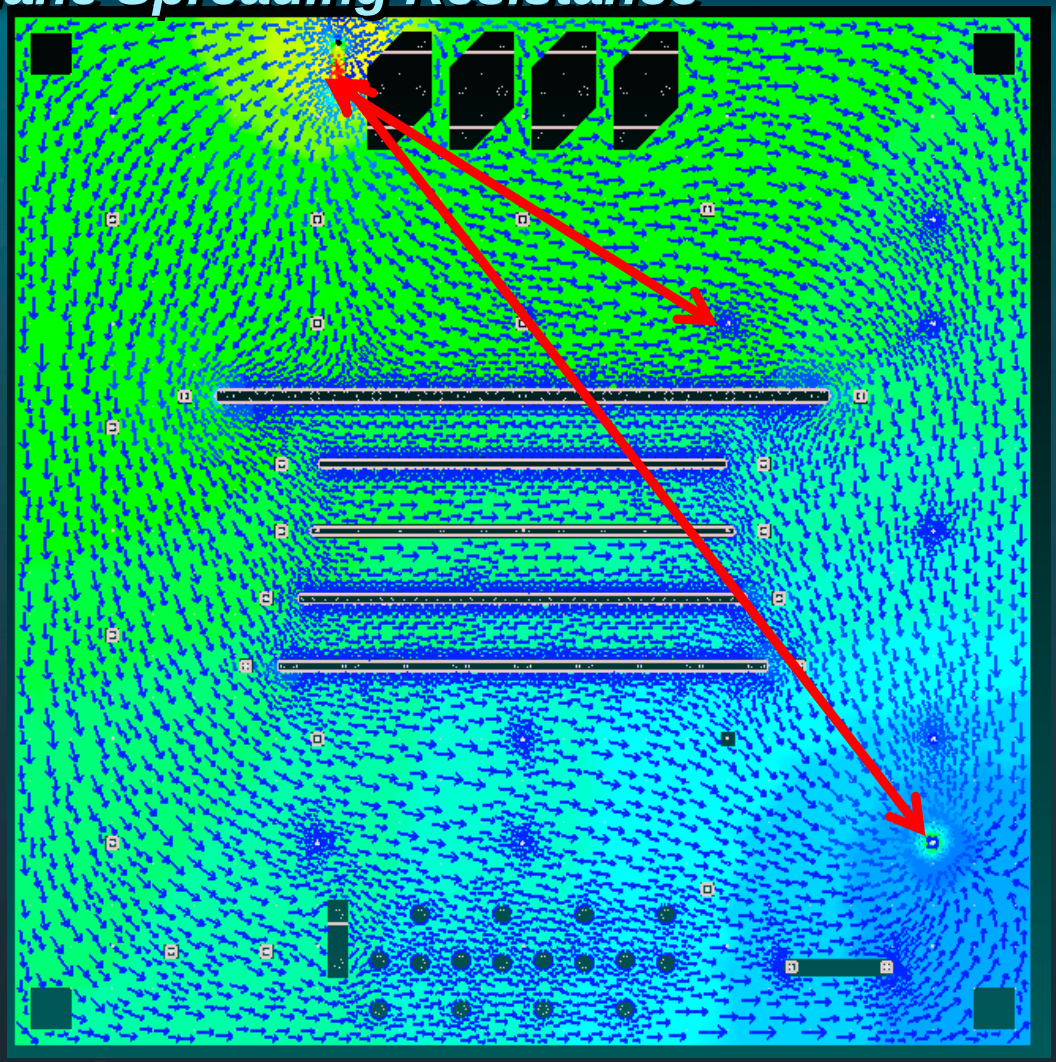
Contact Resistance versus Number of Vias, Via Size, and Spacing



- Spreading resistance decreases with increasing via diameter. However, this exhibits asymptotic behavior.
- Resistance decreases with increased number of vias at constant 100 mil pitch. However, rate of change decreases as via contact density increases.



Measurement to Solver Correlation of Plane Spreading Resistance



Connection Type	Measured vs. Simulated
HPM Short Path	1.19 / 1.25 mΩ
HPM Long Path	1.56 / 1.55 mΩ
HPF Short Path	1.19 / 1.04 mΩ
HPF Long Path	1.69 / 1.54 mΩ

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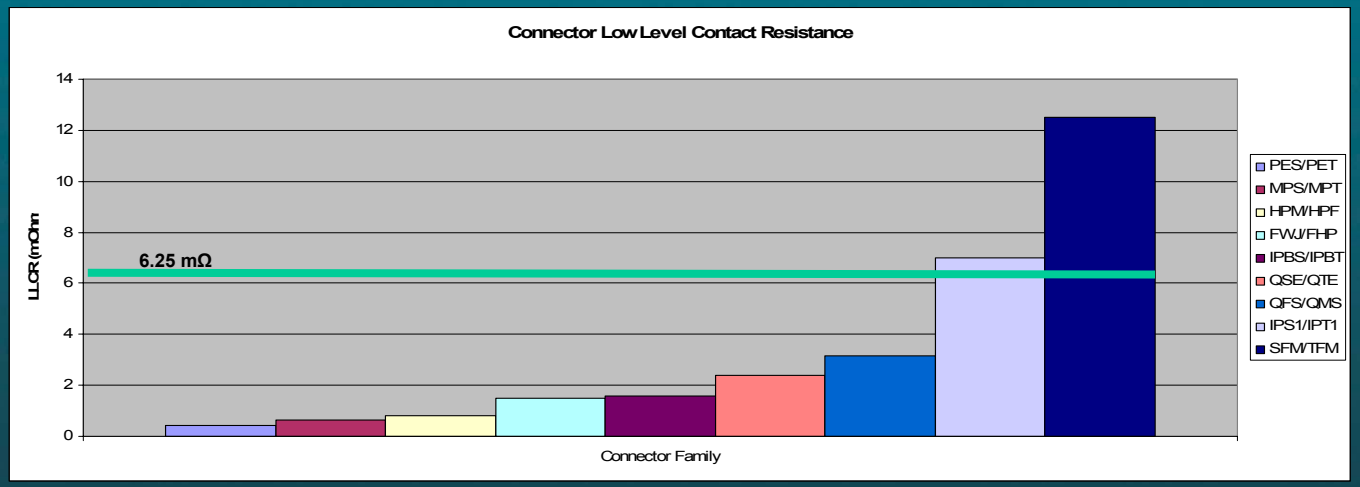
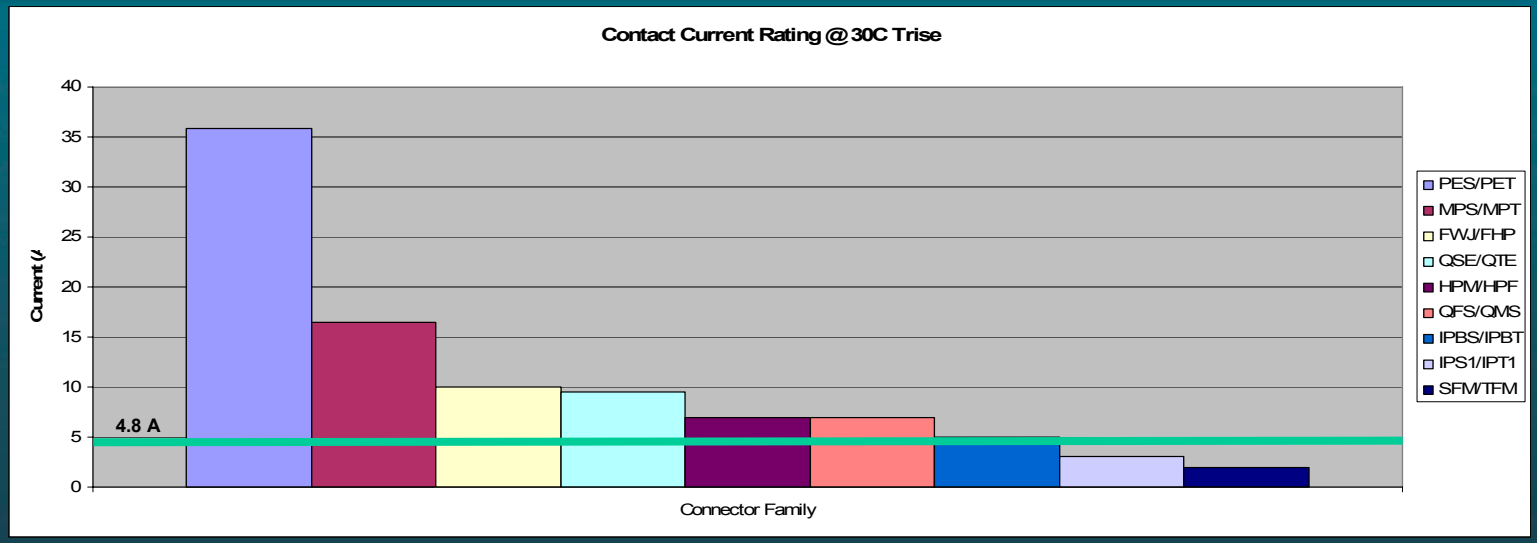
Samtec Connector Low Level Contact Resistance (LLCR)



- **LLCR specifications can be used to quickly determine the suitability of a connector for a particular application.**
  - **Multiple ganged contacts can be used to reduce total resistance.**
    - However, this can be limited by plane spreading resistance.
    - Multiple connector families are well within the 3.125 mΩ per-contact requirement of our example

Samtec Connector Current Rating per Contact



- **Current carrying capacity is the fundamental measure of the "quality factor" of a power connector.**
  - **Designers can use connectors with high current ratings to:**
    - Decrease the number of contacts required
    - Increase reliability and thermal loading with multiple contacts
    - Decrease total path resistance with the fewest number of additional contacts
      - Remember that path resistance is often dominated by plane spreading resistance
  - **A significant number of connector families can meet the 4.8 A total current requirement for the DDR3 example with only 1 contact pair.**
    - But …voltage drop requirements (full path resistance) need to also be considered.

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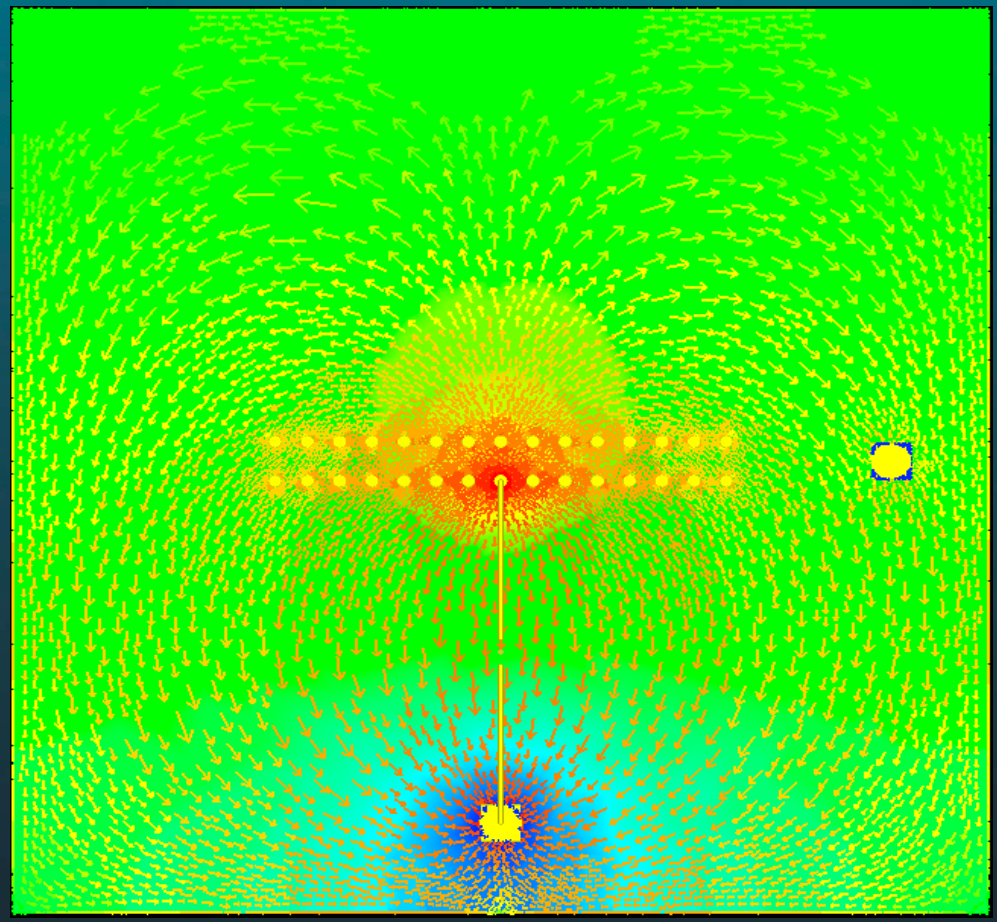
Current/Voltage Density with One Through Hole Power Contact Excited

BOR shows very little degradation of DC current flow into power/ground blade region of connector.

200 mil via used for power delivery to plane, spaced 2” away from connector.

Multiple current sources used to inject 1A current evenly into power blade.



Bottom plane placed 56 mil below top component pads shows worst case via attach resistance for 0.062” boards with internal planes.

55 mil PTH mounting holes.

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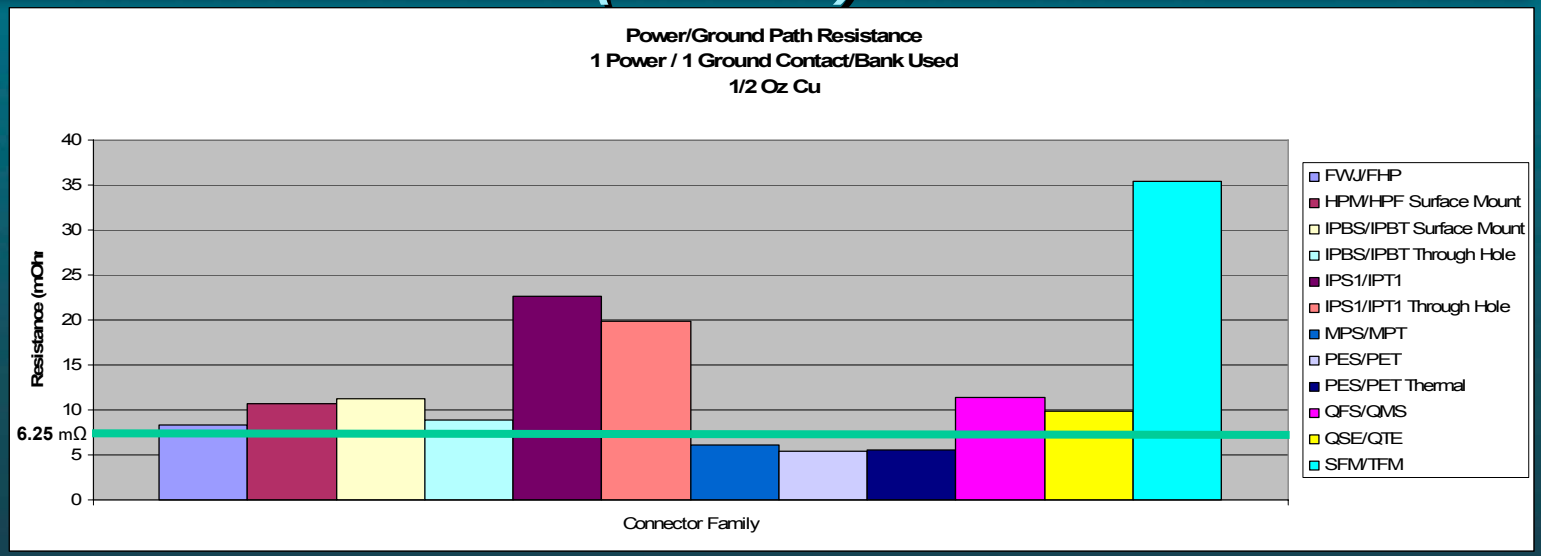
Power/Ground Path Full Path Resistance Example
1 Set of Contacts Excited (½ Oz Cu)



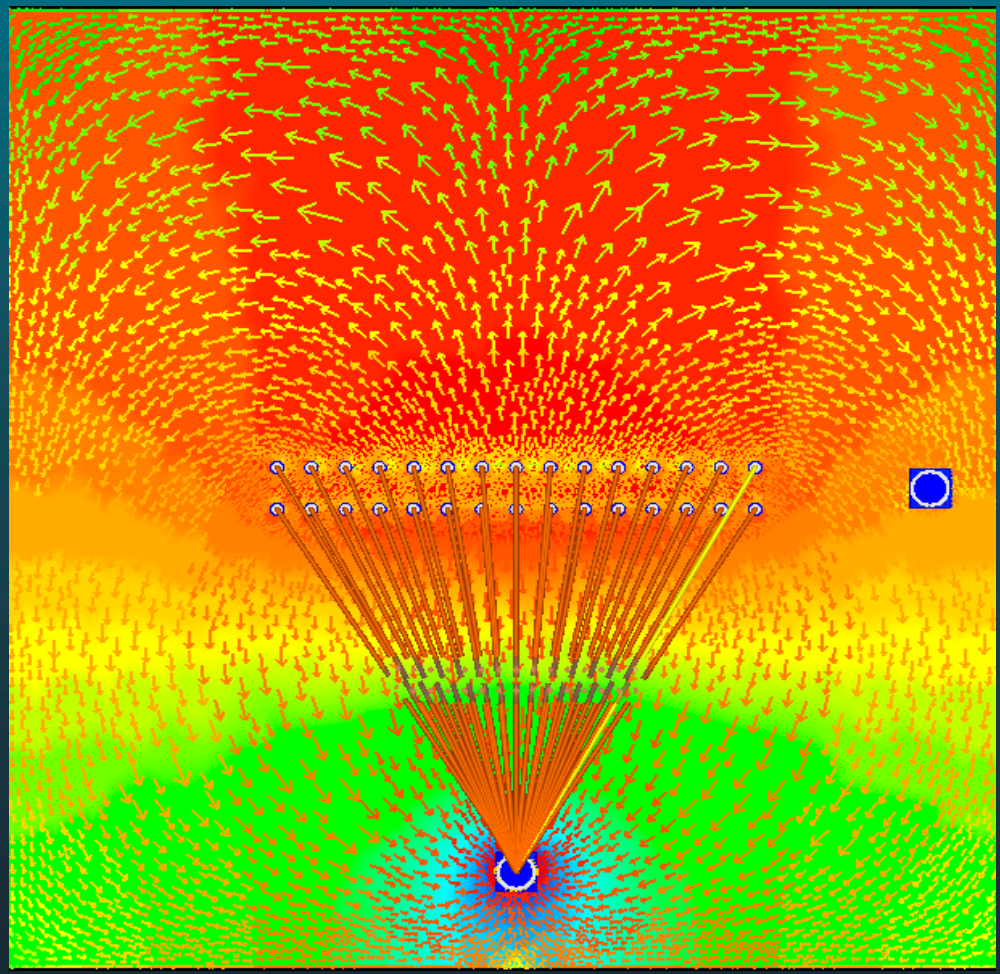
- **Single contact simulations quickly show the relative merits of different connector families.**
  - **For our DDR3 example, only the MPS/MPT and PES/PET connectors meet the 6.25 mΩ path resistance requirement with one pair of contacts on ½ Oz Cu planes.**
    - Multiple contacts are required for other connector systems.
- **Surface mount connectors typically have higher mounted resistance due to current crowding at the BOR vias.**

Current/Voltage Density with Multiple Through Hole Contacts Excited

BOR shows very little degradation of DC current flow into power/ground blade region of connector.

200 mil via used for power delivery to plane, spaced 2” away from connector.

Multiple current sources used to inject 1A current evenly into power blades.



Bottom plane placed 56 mil below top component pads shows worst case via attach resistance for 0.062” boards with internal planes.

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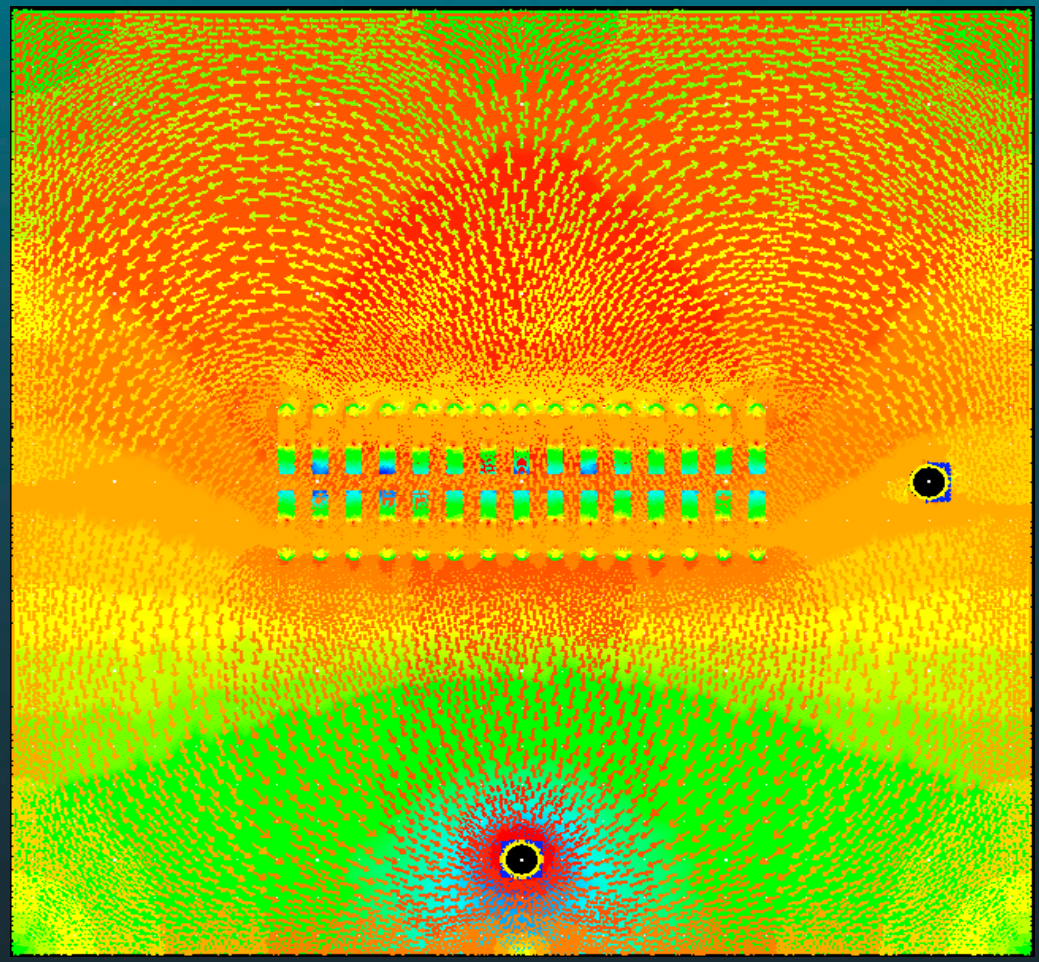
Current/Voltage Density with Multiple Surface Mount Contacts Excited

Surface mount contacts show constriction of current flow at contact vias.

200 mil via used for power delivery to plane, spaced 2” away from connector.

Multiple current sources used to inject 1A current evenly into power blade.



Bottom plane placed 56 mil below top component pads shows worst case via attach resistance for 0.062” boards with internal planes.

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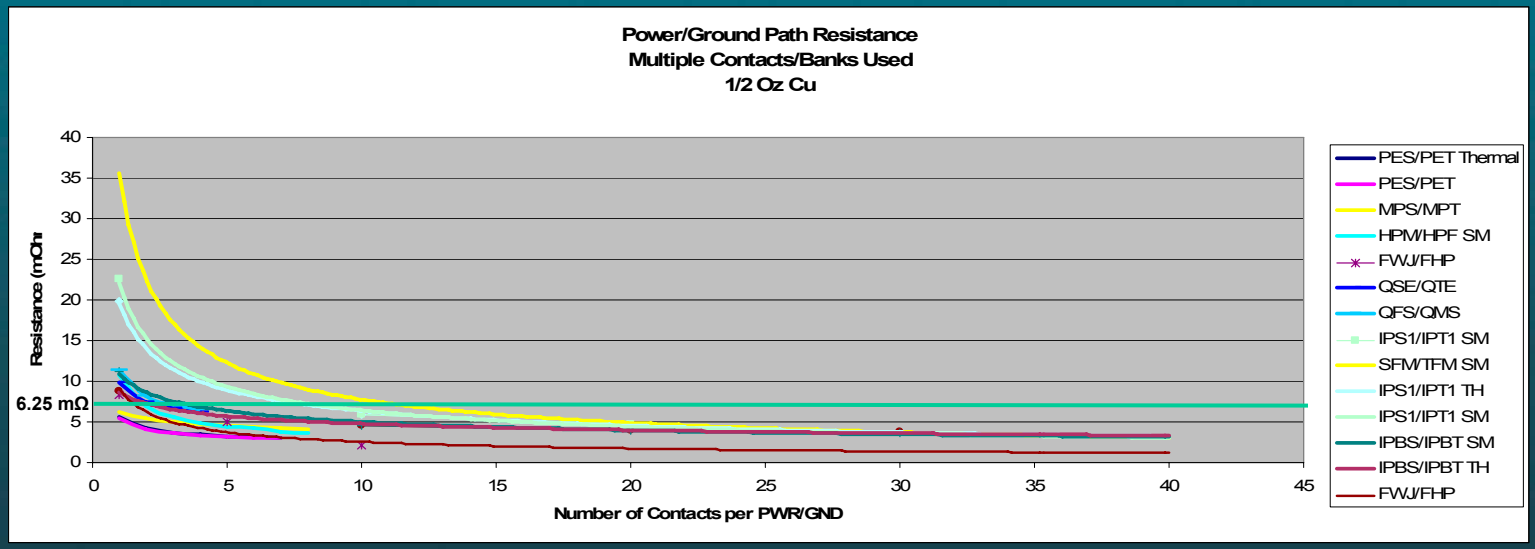
Power/Ground Path Full Path Resistance Example Multiple Sets of Contacts Excited (½ Oz Cu)



- **As multiple contacts are used, overall power delivery resistance is limited by the planes.**
  - **Optimal designs with the smallest space requirements and lowest overall resistance are achieved with low LLCR/High Current connectors**
    - PES/PET, MPS/MPT, FWJ/FHP, HPM/HPF

Summary

- **In this Webinar, we've shown:**
  - **How to analyze the DC margin necessary for a common memory system**
  - **How improving this DC margin can improve AC voltage and timing margins**
  - **How to perform analytical calculations of various power delivery structures**
    - Traces, planes, and vias
  - **Why DC solvers may required for the complex geometry seen in most real power delivery systems**
  - **How plane spreading resistance (current crowding) impacts DC resistance**
  - **How to evaluate connector specifications**
    - LLCR and Current Ratings
  - **Why the full PCB/Connector system must be evaluated to guarantee performance**

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Thank You

- Thank you for your participation in today's webinar presentation. If you have any questions, please feel free to contact our Power Integrity Group at PIgroup@samtec.com.
- Contact us at ewebinar@samtec.com to receive a copy of today's presentation.